

MPT11220IL Power Module

Wide Input Voltage Range, 20A Buck Converter with Integrated Inductor

Description

The MPT11220IL Power Module is a high efficiency, synchronous step-down (Buck) DC-DC converter capable of delivering 20A continuous current. The MPT11220IL is an advanced 11mm x 17mm x 6.21mm 100-pin open frame package, that integrates an inductor, MOSFET switches, small-signal circuits, and compensation.

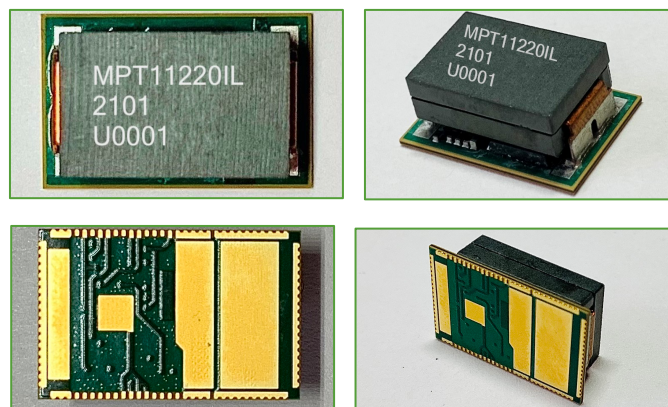
The MPT11220IL Power Module operates over a wide input voltage range of 4.5V to 16V and applies a Constant-On-Time (COT) control scheme which provides very fast load transient response and easy loop design. It integrates full protection features, including short-circuit protection, over-current protection, under voltage protection, and thermal shutdown to make the part operate safely.

The MPT11220IL Power Module requires a minimal number of readily available, standard, external components which significantly helps in system design and productivity by offering greatly simplified board design, layout, and manufacturing requirements. In addition, a reduction in the number of components required for the complete power solution helps to enable an overall system cost saving. The MPT11220IL Power Module is RoHS compliant and lead-free manufacturing environment compatible.

Features

- Excellent Ripple and Transient Performance
- Up to 20A Continuous Operating Current
- Wide 4.5V to 16V VIN range
- 0.6V to 5.0V VOUT range
- Optimized Solution Size
- Programmable switching frequency range from 600kHz to 1.2MHz
- Easy compensation with a single resistor
- Thermal, Over-Current, Short Circuit, Under-Voltage, and Pre-Bias Protections
- Pb-Free and RoHS Compliant, MSL Level 3, 260°C Reflow

Module Form Factor



11x17mm Open-Frame Package

Applications

- FPGAs, ASICs, DSPs, Network processors, Industrial applications
- High density double data rate (DDR) memory VDDQ rails
- Server Power Systems
- High Thermal requirement applications

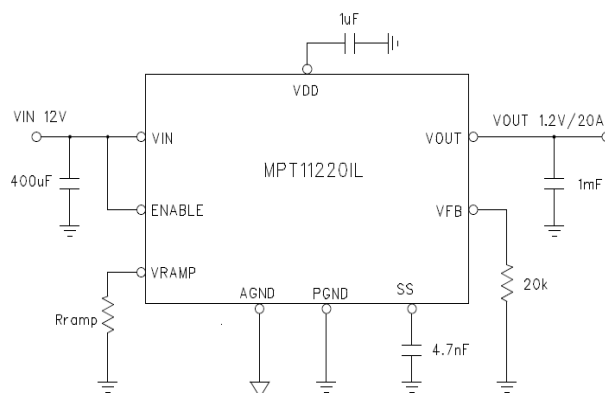


Figure 1: Simplified Applications Circuit

Ordering Information

| Part Number | Package Marking | T _A Rating | Package Description |
|----------------|-----------------|-------------------------------|---|
| MPT11220IL | MPT11220IL | -40°C ≤ T _A ≤ 85°C | 11mm x 17mm x 6.21mm 100-pin Open-Frame |
| MPT11220IL-EVB | MPT11220IL | Customer Evaluation Board | |

Pin Functions

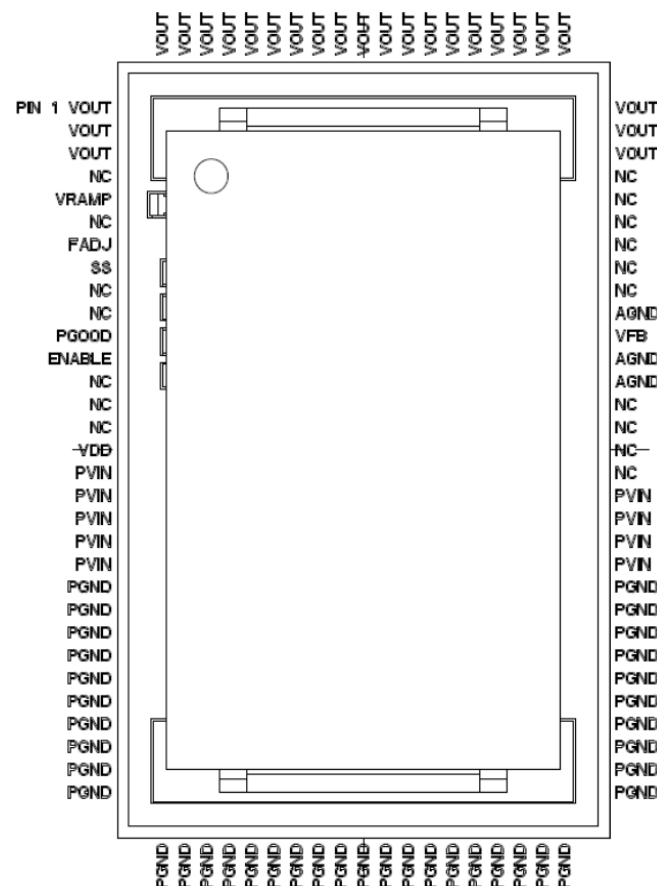


Figure 2: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Functions (Continued)

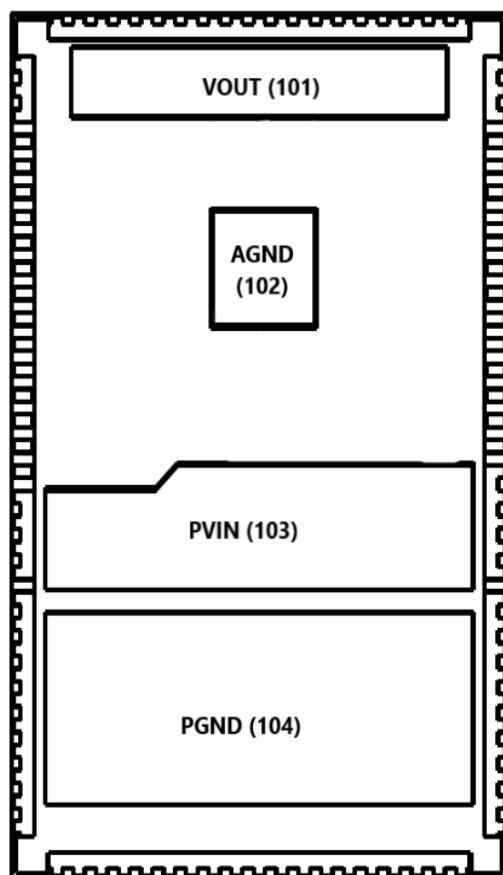


Figure 2A: Pin Diagram (Bottom View)

Pin Descriptions

| PIN | NAME | FUNCTION |
|---------------------------------------|--------|--|
| 4,6,9,10,13 - 15, 65 - 68, 73 - 78 | NC | No Connect. These pins must be soldered to PCB but not electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage. |
| 1 – 3, 79 – 100, 101 | VOUT | Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and GND pins. Refer to the Layout Recommendation section for more details. |
| 22 – 60, 104 | PGND | Input/Output power ground. Connect to the ground electrode of the input and output filter capacitors. Refer to the Layout Recommendation section for more details. |
| 69,70,72, 102 | AGND | Analog ground. Connect to system ground plane. Refer to the Layout Recommendation section for more details. |
| 17 – 21, 61 – 64, 103 | PVIN | Input power supply. Connect to input power supply. Decouple with input capacitor to GND pin. Refer to the Layout Recommendation section for more details. |
| 5 | VRAMP | Connect a resistor between VRAMP pin and GND to set the compensation. |
| 7 | FADJ | Frequency adjust pin. Connect a resistor between FADJ pin and GND to set the switching frequency. Frequency can be programmed from 600KHz to 1.2MHz. |
| 8 | SS | Soft start control input pin. This pin is used to program the soft start period with an external capacitor connected to GND. |
| 11 | PGOOD | Power good indication pin. It's an open drain output. It will pull low when over current, short circuit, over temperature, UVLO, UVP, and output voltage loss of regulation, including output pre-bias. |
| 12 | ENABLE | Enable pin. Applying logic high to the ENABLE pin will enable the device and initiate a soft-start. Applying logic low disables the output and switching stops. ENABLE can be connected to VIN directly or through a resistor. There's an internal 2uA pull up current source. |
| 16 | VDD | Internal 5.45V LDO output. Connect a 1uF capacitor from VDD to GND. |
| 71 | VFB | External feedback input pin. Connect a resistor between VFB and GND, and another resistor between VFB to VOUT to set the output voltage. Refer to the Output Voltage Setting section for more details. |

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|----------------|----------------------------------|------|---------------|-------|
| Input Voltage | PVIN | -0.3 | 18 | V |
| Device Enable | ENABLE | -0.3 | $PV_{IN}+0.3$ | V |
| All Other Pins | VRAMP, FADJ, SS, PGOOD, VDD, VFB | -0.3 | 6 | V |

Absolute Maximum Thermal Ratings

| PARAMETER | CONDITION | MIN | MAX | UNITS |
|--|--------------------------------|-----|------|-------|
| Maximum Operating Junction Temperature | | | +150 | °C |
| Storage Temperature Range | | -65 | +150 | °C |
| Reflow Peak Body Temperature | (10 Sec) MSL3 JEDEC J-STD-020A | | +260 | °C |

Absolute Minimum ESD Ratings

| PARAMETER | CONDITION | MIN | MAX | UNITS |
|----------------------------|-----------|-------|-----|-------|
| HBM (Human Body Model) | | ±2000 | | V |
| CDM (Charged Device Model) | | ±500 | | V |

Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | MAX | UNITS |
|--------------------------------|-----------|-----|-----------|-------|
| Input Voltage Range | PV_{IN} | 4.5 | 16.0 | V |
| Device Enable pin Voltage | Enable | 0 | PV_{IN} | V |
| Output Voltage Range | V_{OUT} | 0.6 | 5.0 | V |
| Output Current Range | I_{OUT} | 0 | 20 | A |
| Operating Junction Temperature | T_J | -40 | +125 | °C |

Thermal Characteristics

| PARAMETER | SYMBOL | TYPICAL | UNITS |
|--|---------------|---------|-------|
| Thermal Shutdown | T_{SD} | 150 | °C |
| Thermal Shutdown Hysteresis | T_{SDHYS} | 15 | °C |
| Thermal Resistance: Junction to Ambient (0 LFM) ⁽¹⁾ | θ_{JA} | 4.8 | °C/W |

(1) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

Electrical Characteristics

NOTE: $V_{IN} = 12V$, Minimum and Maximum values are over operating ambient temperature, V_{IN} , and load range unless otherwise noted. Typical values are at $T_a = 25^\circ C$.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|----------------|--|-------|------|-------|----------|
| Operating Input Voltage ⁽¹⁾ | PV_{IN} | | 4.5 | | 16.0 | V |
| Under Voltage Lock-Out – V_{IN} Rising | V_{UVLOR} | Voltage above which UVLO is not asserted | 4.1 | 4.3 | 4.5 | V |
| Under Voltage Lock-Out – V_{IN} Falling | V_{UVLOF} | Voltage below which UVLO is asserted | | 3.3 | | V |
| Under Voltage Lock-Out Hysteresis | $V_{UVLOHYS}$ | | | 1 | | V |
| Vout Over Voltage Protection | V_{OVPR} | VFB rising | | 117 | | % |
| OVP Hysteresis | $V_{OVP-HYST}$ | VFB falling | | 2.5 | | % |
| Vout Under Voltage Protection | V_{UVPF} | VFB falling | | 94 | | % |
| UVP Hysteresis | $V_{UVP-HYST}$ | VFB Rising | | 3 | | % |
| Shut-Down Supply Current | I_S | ENABLE = 0V | | | 10 | μA |
| No Load Quiescent Current | I_{VINQ} | $V_{OUT} = 1.2V$ | | 4.3 | | mA |
| Internal LDO output | V_{DD} | 25mA load, T_a from $-40^\circ C$ to $85^\circ C$ | 5.35 | 5.45 | 5.55 | V |
| Feedback Pin Voltage ⁽²⁾ | V_{FB} | $V_{OUT} = 0.6V$, $I_{LOAD} = 0$, $T_a = 25^\circ C$ | 0.594 | 0.6 | 0.606 | V |
| Feedback Pin Voltage (Line, Load, Temp.) | V_{FB} | $4.5V \leq PV_{IN} \leq 16.0V$ $0A \leq I_{LOAD} \leq 20A$; $-40^\circ C \leq T_a \leq 85^\circ C$ | 0.588 | 0.6 | 0.612 | V |
| Feedback pin Input Leakage Current ⁽³⁾ | I_{FB} | VFB pin input leakage current | -50 | | 50 | nA |
| Soft start source current | I_{SS} | SS=0V, T_a from $-40^\circ C$ to $85^\circ C$ | 3 | 4 | 5 | μA |
| Soft start pulldown resistance | R_{SS} | SS=0.8V | | 80 | | Ω |
| V_{OUT} Rise Time ⁽³⁾ | t_{RISE} | | | 1 | | ms |
| Continuous Output Current | I_{OUT} | | 0 | | 20 | A |
| Current Limit Trip Level | I_{OCP} | $V_{IN} = 12V$, $V_{OUT} = 1.2V$, T_a from $-40^\circ C$ to $85^\circ C$ | 30 | 36 | | A |
| Current Limit Retry Time ⁽³⁾ | T_{CL_TRY} | | | 2.5 | | ms |
| Disable Threshold | $V_{DISABLE}$ | ENABLE pin logic going low | | 1.1 | | V |
| Enable Threshold | V_{EN} | ENABLE pin logic going high | 1.18 | 1.2 | 1.4 | V |
| Enable Hysteresis | EN_{HYS} | | | 100 | | mV |
| Enable Internal Pullup Current | I_{EN} | EN = 0V | | 2 | | μA |
| PGOOD pulldown resistance | R_{PG} | PGOOD=0.1V | | 100 | | Ω |
| Switching Frequency | F_{SW} | Programmable Switching frequency | 580 | | 1300 | kHz |

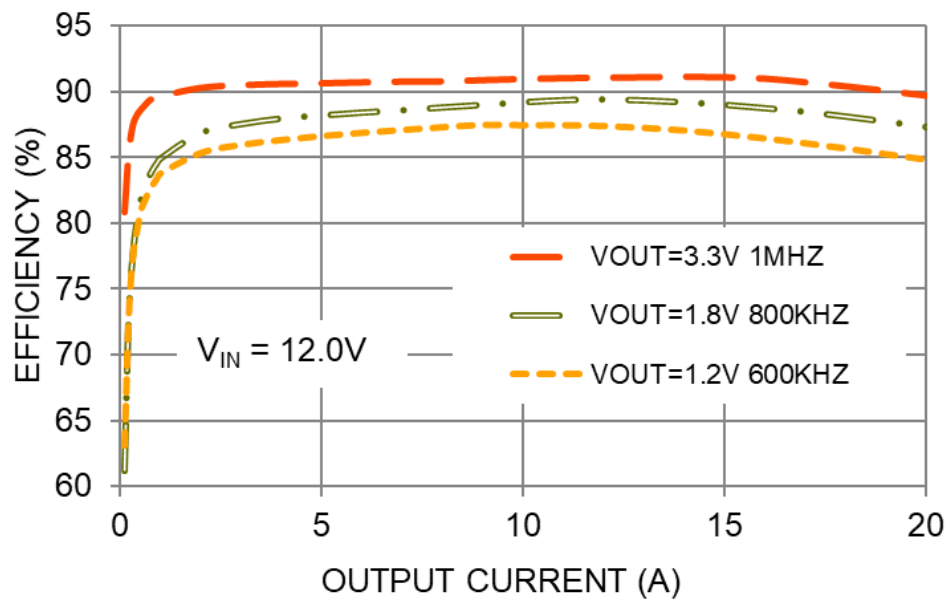
⁽¹⁾ Minimum V_{IN} voltage must be at least 1.3V higher than V_{out} .

⁽²⁾ The FB pin is a sensitive node. Do not touch FB while the device is in regulation.

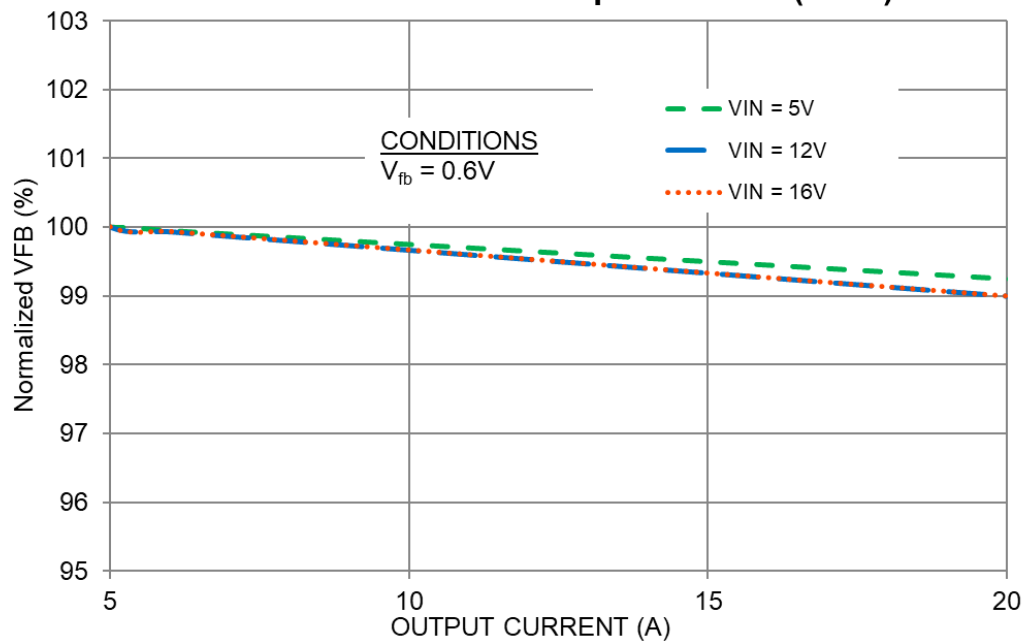
⁽³⁾ Parameter not production tested but is guaranteed by design.

Typical Performance Curves

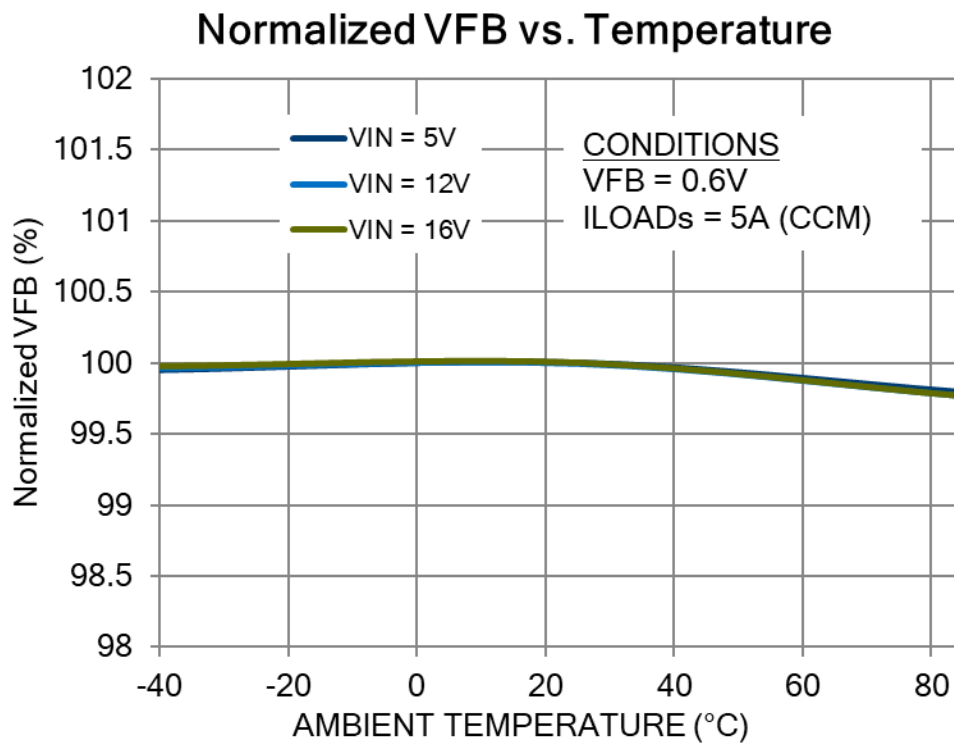
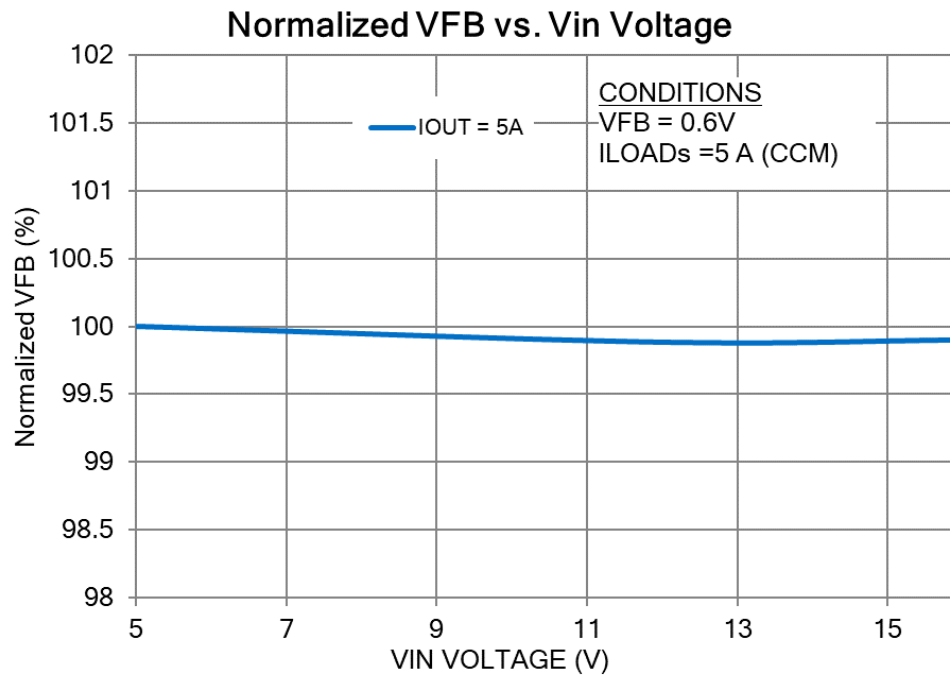
Efficiency vs. Output Current



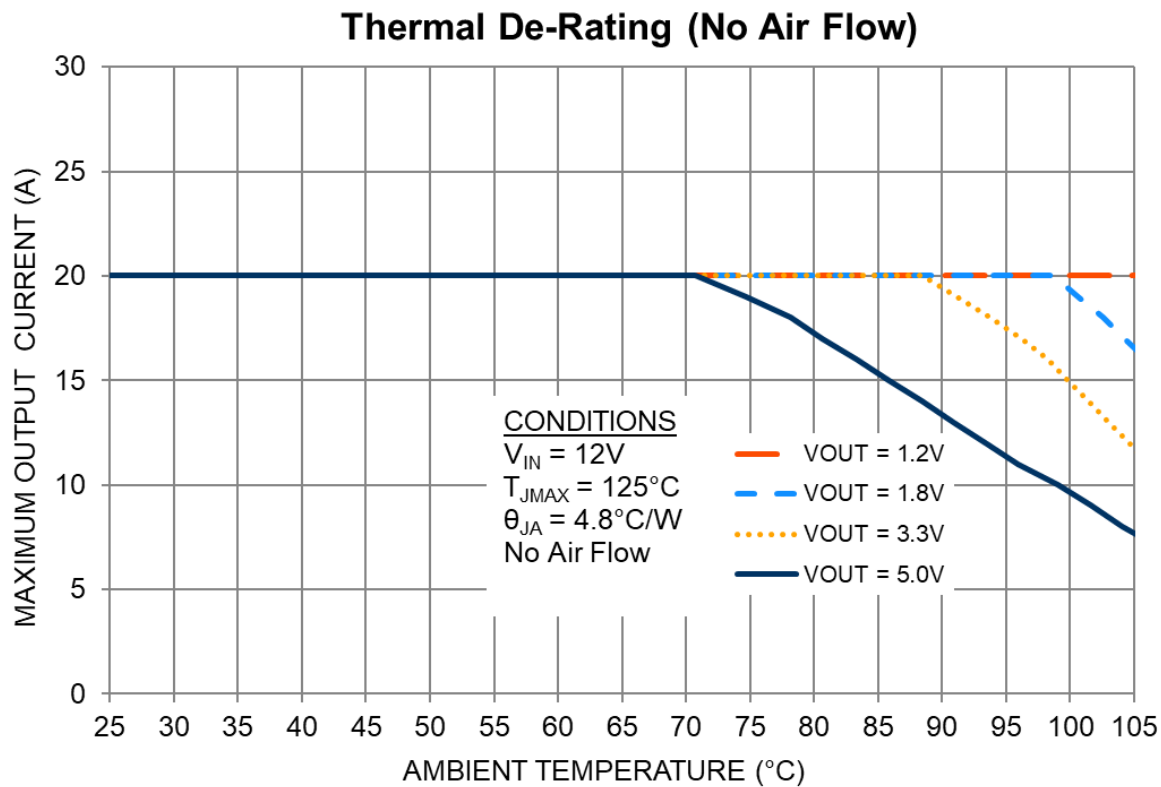
Normalized VFB vs. Output Current (CCM)



Typical Performance Curves (Continued)

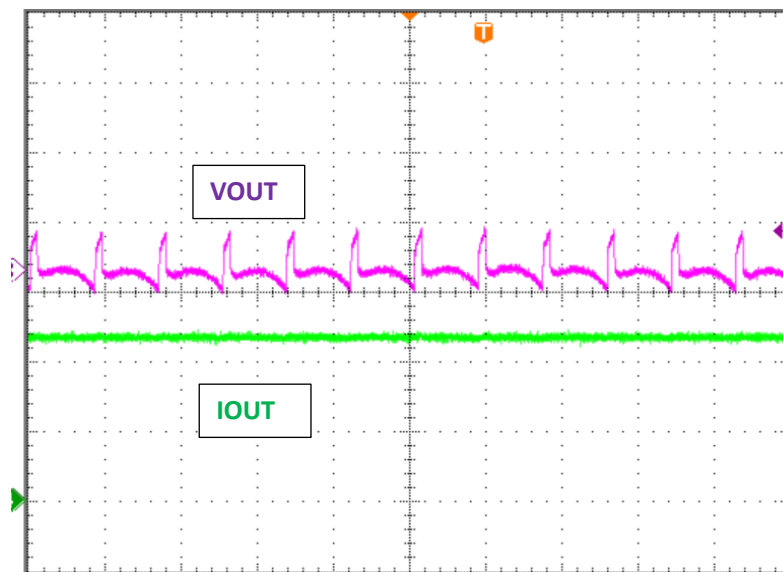


Typical Performance Curves (Continued)



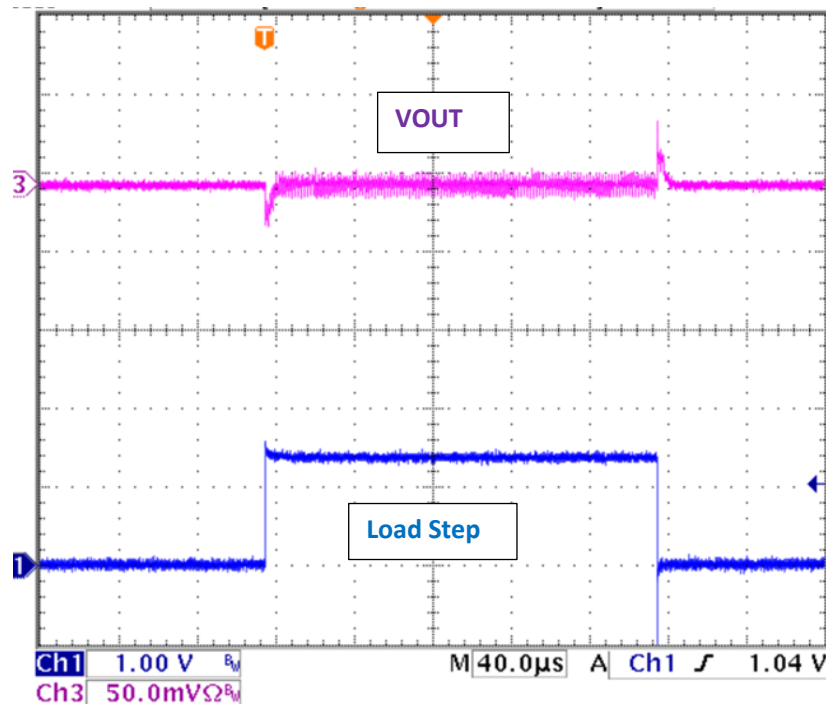
CAUTION: Functional operation beyond the recommended maximum operating junction temperature of 125°C may impair device life. Exposure to this condition for extended periods may affect device reliability. The de-rating curves are based on device mounted on PCBs with 2oz. external copper layers and proper thermal design in line with EII/JEDEC JESD51-7 standard for high thermal conductivity boards.

Typical Performance Characteristics



Output Voltage Ripple, 20A Output Current

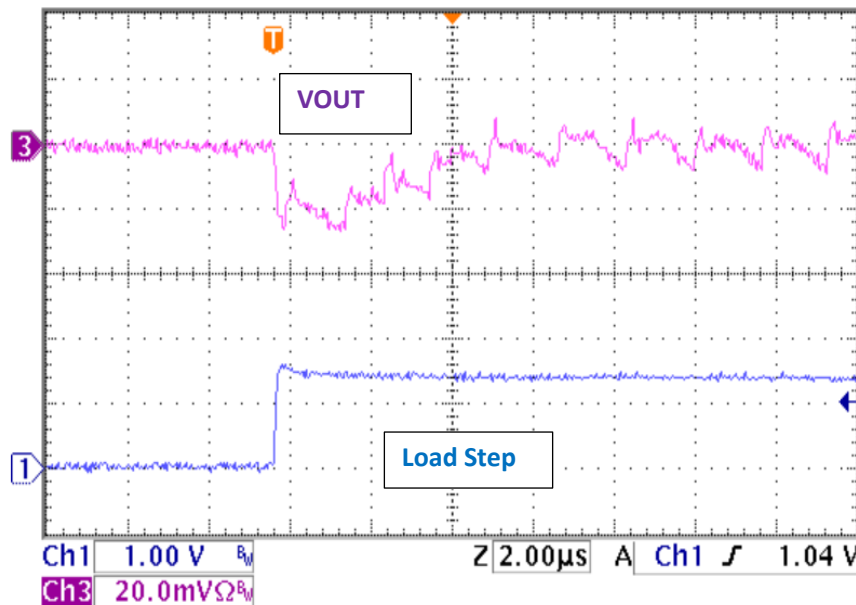
$V_{in} = 12V$, $V_{out} = 1.2V$, $2 \mu S/div$, $V_{out} : 5 mV/div$, 20MHz Bandwidth



Output Voltage Load Transient Response, Load Step = 0A to 20A

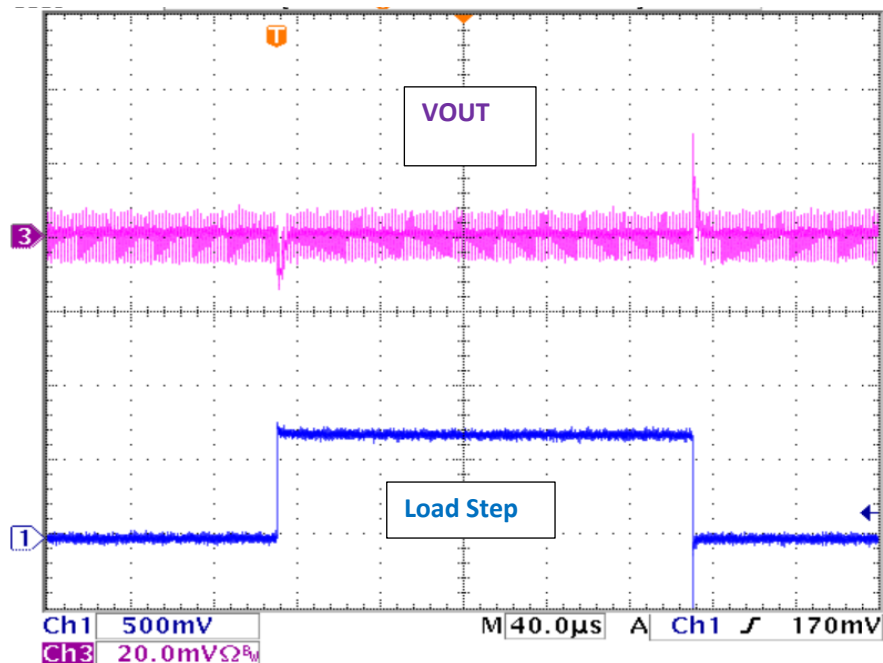
$V_{in} = 12V$, $V_{out} = 1.2V$, $40 \mu S/div$, $V_{out} : 50mV/div$, $C_{out}=1mF$

Typical Performance Characteristics (Continued)



Output Voltage Load Transient Response, Load Step = 0A to 20A

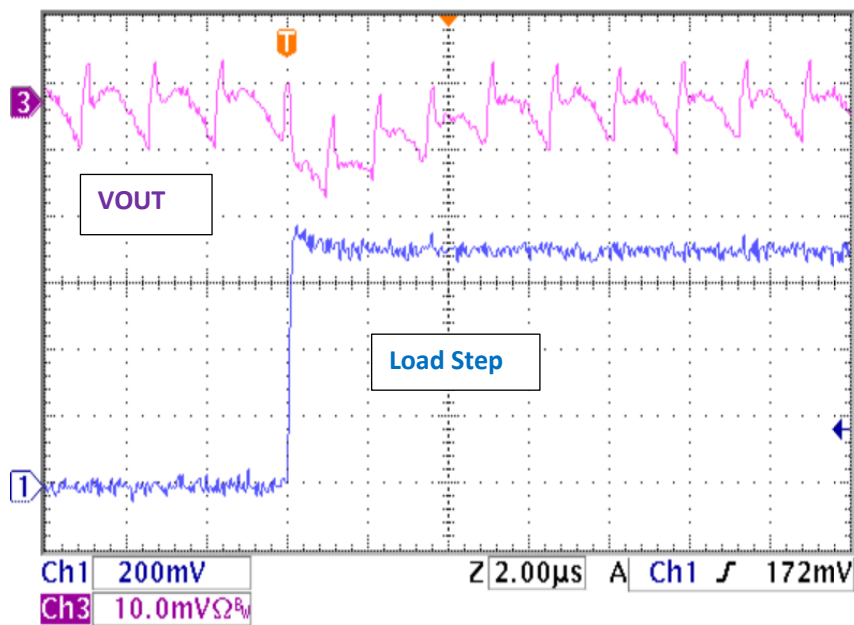
$V_{in} = 12V$, $V_{out} = 1.2V$, $2\mu S/div$, $V_{out} : 20mV/div$, $C_{out}=1mF$



Output Voltage Load Transient Response, DC Load = 10A, Load Step = 10A to 20A

$V_{in} = 12V$, $V_{out} = 1.2V$, $40\mu S/div$, $V_{out} : 20mV/div$, $C_{out}=1mF$

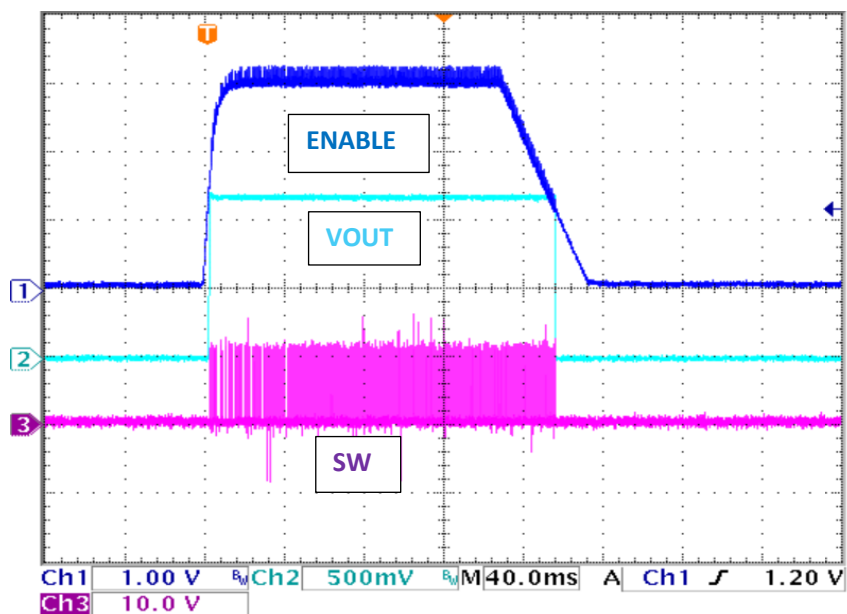
Typical Performance Characteristics (Continued)



Output Voltage Load Transient Response, DC Load = 10A, Load Step = 10A to 20A

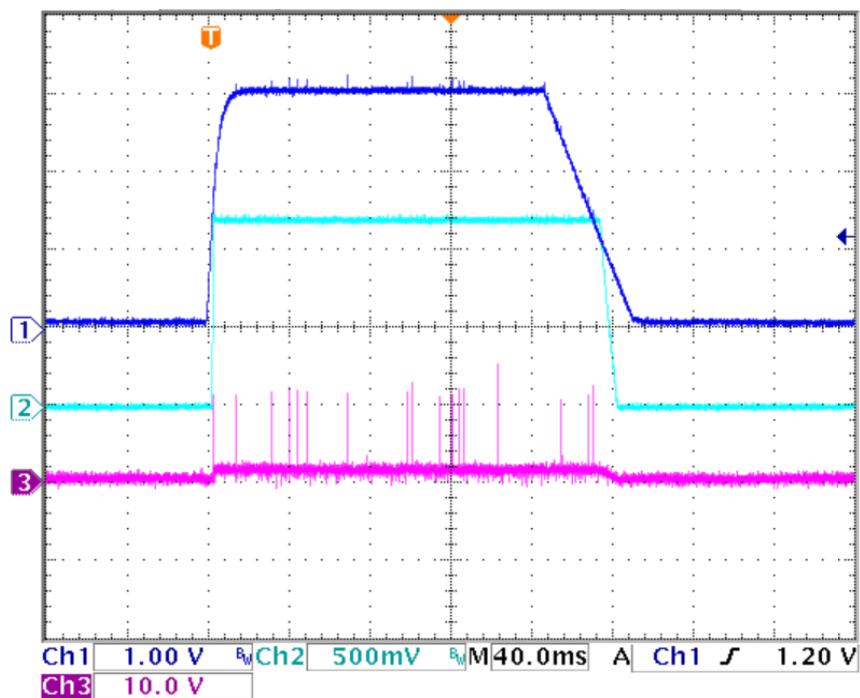
$V_{in} = 12V$, $V_{out} = 1.2V$, 2 μ S/div, $V_{out} : 10mV/div$, $C_{out} = 1mF$

Typical Performance Characteristics (Continued)



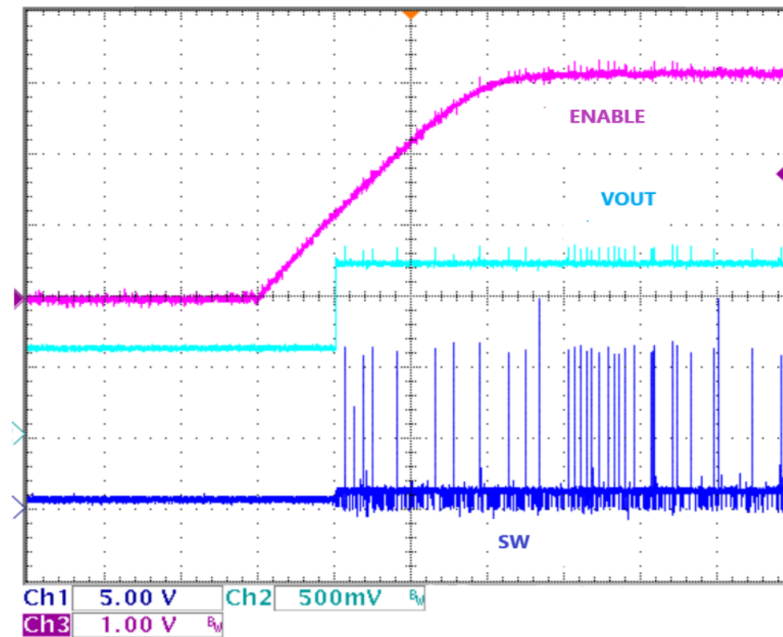
Enable / Disable, Load = 20A

Vin = 12V, Vout = 1.2V



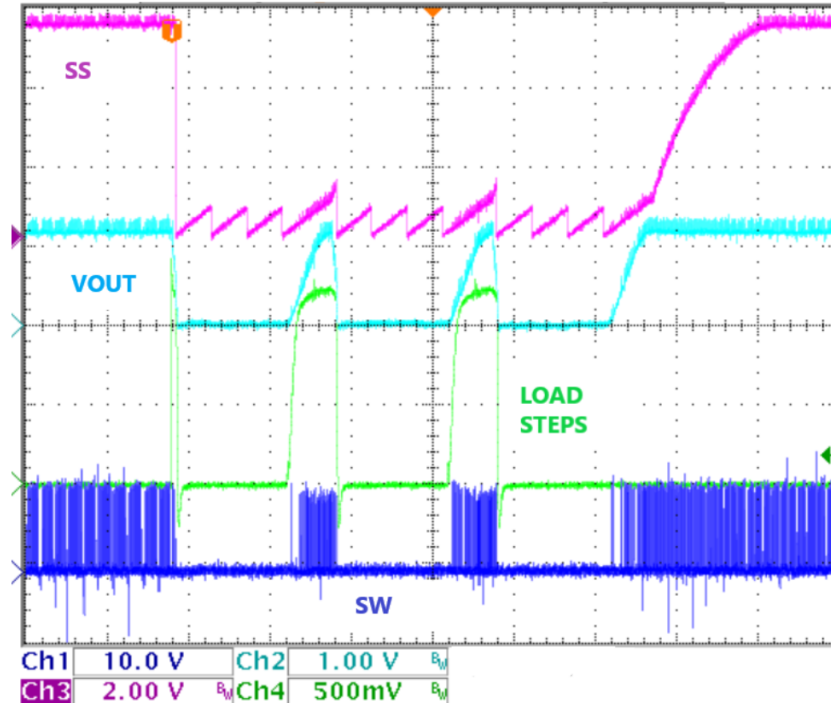
Short Circuit RECOVERY, 12V Vin, 1.2V Vout

Typical Performance Characteristics (Continued)



ENABLE Startup from Pre-Bias of 0.6V, Load = 0A

Vin = 12V, Vout = 1.2V



Hiccup Mode from OCP event, DC Load = 10A, Load Step = 10A to 30A

Vin = 12V, Vout = 1.2V, 2mS/div

Functional Block Diagram

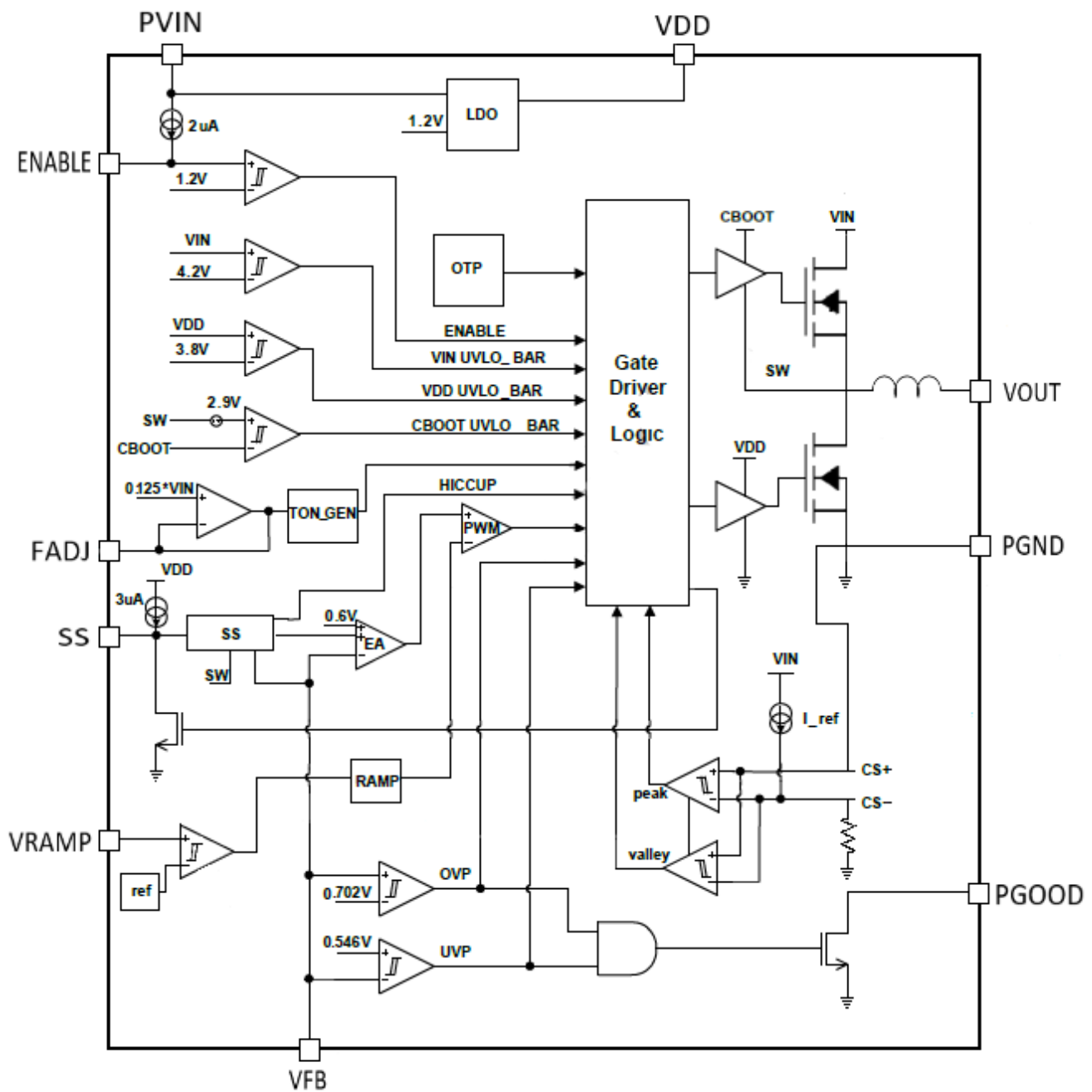


Figure 3: Functional Block Diagram

Functional Description

The MPT11220IL is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and to simplify loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the FB voltage (VFB) drops below the reference voltage (VREF). The HS-FET is turned on for a fixed interval determined by the one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range. After the on period elapses, the HS-FET is turned off until the next period begins. By repeating this operation, the converter regulates the output voltage. Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps. The low side MOSFET is turned on when the high side MOSFET is in its off state to minimize conduction loss. To prevent a shoot-through (a short between the input and GND if both the HS-FET and LS-FET are turned on at the same time), a dead time is generated internally between the HS-MOSFET off and LS-MOSFET on, or LS-MOSFET off and HS-MOSFET on.

When the MPT11220IL works in PFM mode during light-load operation, the MPT11203IQ reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side driver enters tri-state (high-Z). The output capacitors discharge slowly to GND through FB divider resistors. When VFB drops below the reference voltage, the HS-FET is turned on. This operation improves device efficiency greatly when the output current is low. During Light-load operation, the HS-FET does not turn on as frequently as it does in heavy-load conditions.

The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero, and can be determined with Equation (1):

$$I_{out} = \frac{(V_{in} - V_{out}) \times V_{out}}{2 \times L \times F_{sw} \times V_{in}}$$

The MPT11220IL reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Internal LDO (VDD)

An internal LDO (VDD) with a 5.45V voltage output provides power for the gate drivers and bootstrap circuit. If PVIN is lower than VDD, the LDO will try to regulate its output voltage equal to PVIN. The LDO has current limit protection, typically is 120mA.

Enable Control (ENABLE)

Enable is a digital control pin that turns the converter on and off. Drive ENABLE high to turn on the converter. Drive ENABLE low to turn off the converter. It uses a bandgap generated precision threshold of 1.2V. There is a 2uA internal pull up current at ENABLE terminal. Moreover, ENABLE pin voltage can tolerate as high as PVIN, so user can tie ENABLE to PVIN directly if MPT11220IL is always enable needed.

Functional Description (Continued)

Programmable Switching Frequency (FADJ)

The Switching Frequency can be programmed to optimize efficiency and ripple currents over the various ranges for Vout and Vin. There are a number of variables to consider when choosing the switching frequency. A high frequency will increase switching losses and gate charge losses, while a lower frequency requires more inductance and capacitance to offset larger inductor ripple current, which results in larger real estate and also higher cost. It is a trade-off between power loss and passive component size. Additionally, in noise-sensitive applications, the switching frequency should be out of a sensitive frequency band. The switching frequency can be programmed from 600KHz to 1.2MHz with resistor between FADJ and GND. Please see the recommended Switching Frequency vs. Output voltage setting in the graph below:

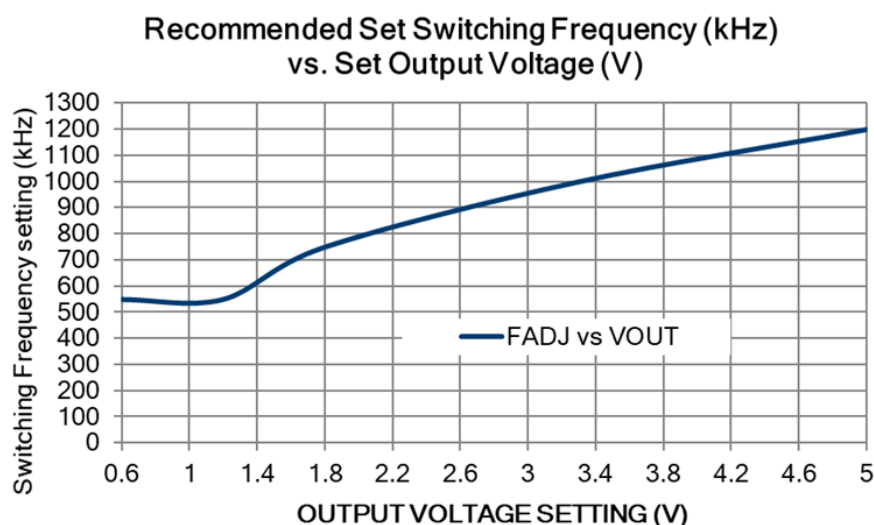


Figure 4: Recommendation chart for Fsw and associated Output Voltage setting

Loop Compensation (VRAMP)

The MPT11220IL uses constant on time (COT) control mode which makes the loop compensation easy. By connecting a resistor between VRAMP and GND, the amplitude of the internal ramp generator in the control loop can be adjusted to make the system less sensitive to noise and more stable. The drawback to larger VRAMP, however, will also make load transient response worse. There are 8 settings for VRAMP to account for Light load Mode operation. Please refer to Application Information section for VRAMP resistor settings.

Under Voltage Lock Out (UVLO)

Under-voltage lock out protection (UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, typically 3.7V, the device is shut down. The rising threshold is typically 4.2V.

Functional Description (Continued)

VOUT OVP/UVI Detection and Power Good Indication

VOUT voltage is precisely monitored by VFB voltage. If VFB voltage is typically 17% higher than the internal reference voltage, the MPT11220IL will recognize it as an output over voltage event. Once it triggers OVP, both HS-FET and LS-FET are turned off. MPT11220IL works at this mode until the over-voltage condition is cleared. If VFB voltage is typically 6% lower than reference voltage, MPT11220IL will recognize it as an output under voltage event, UVP. The PGOOD pin will be pulled low after 20 μ s delay when either OVP or UVP case happens.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The MPT11220IL has valley current-limit control. During LS-FET on, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the LS-MOSFET limit comparator turns over. The device enters over current protection (OCP) mode and the HS-FET waits until the valley current limit disappears before turning on again. The output voltage drops until VFB is below the under voltage (UV) threshold (typically 44% below the reference). Once UV is triggered, the MPT11220IL enters hiccup mode to restart the part periodically. During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels.

Soft Start and Pre-Biased Soft Start (SS)

The soft start (SS) is implemented to prevent the converter output voltage from overshooting during startup. During startup, the internal circuitry generates a soft-start voltage ramping up from 0V to 0.6V. When it is lower than internal reference voltage, SS voltage overrides the reference voltage, so the error amplifier uses SS voltage as the reference. When SS voltage is higher than the reference, then the reference regains control.

An external capacitor connected from SS to GND is charged from an internal 3 μ A current source, producing a ramped voltage. The soft start time is set by the external SS capacitor and can be calculated by $T_{SS} = 0.6 \cdot C_{SS} / 3\mu A$ if soft start time is longer than 1ms. Where C_{SS} is the external SS capacitor, and I_{SS} is the 3 μ A SS charge current. There is an internal 1ms soft start timer.

Thermal-Shutdown

Thermal shutdown prevents the converter from operating at exceedingly high temperatures. The converter monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), the converter shuts off. When the temperature is lower than its lower threshold, typically 135°C, the converter starts up again.

Application Information

Output Voltage Setting

The MPT11220IL output voltage is programmed by setting two resistors, one resistor between FB and VOUT (R1) and one resistor between FB and GND (R2). Figure 5 shows the resistor configuration. It is recommended to use 20kΩ for R1 and adjust R2 to set the output voltage.

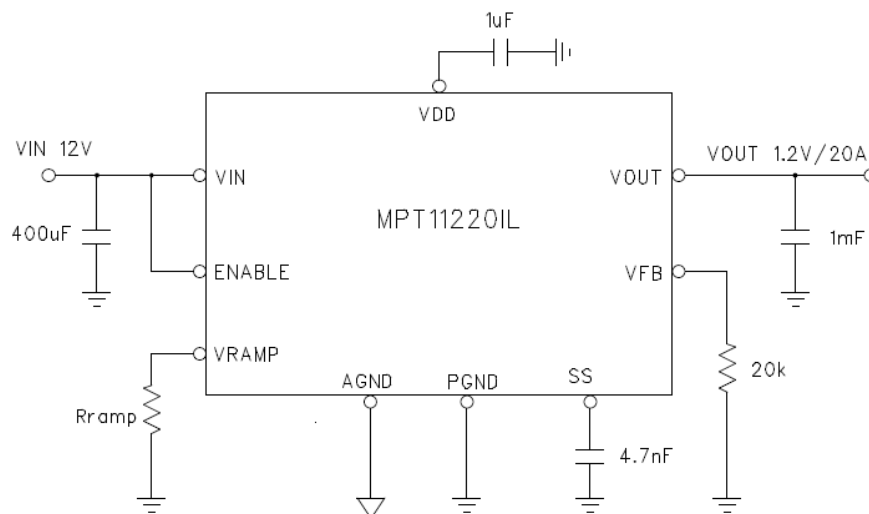


Figure 5: Typical Applications Circuit

Depending on input and output voltage, the recommended external passive component values are shown in Table 1.

| V _{IN} | V _{OUT} | R ₁ | R ₂ | C _{OUT} |
|-----------------|------------------|----------------|----------------|------------------|
| 12V | 0.6V | 20kΩ | OPEN | 1mF |
| | 1.2V | 20kΩ | 20kΩ | |
| | 1.8V | 20kΩ | 10kΩ | |
| | 3.3V | 20kΩ | 4.42kΩ | |
| | 5.0V | 20kΩ | 2.74kΩ | |

Table 1: Common external passive component settings

Setting other Output Voltages

To choose output voltage settings other than those stated in table 1, assume R1= 20kΩ, choose resistor between FB and GND (R2), per the formula below:

$$R2 = \frac{12}{VOUT - 0.6}$$

Application Information (Continued)

Input Capacitor Selection

The input of a synchronous buck converter can be very noisy due to the discontinuous nature of the input current. Therefore, it is necessary to decouple the input properly in order to ensure stable operation. In addition, input parasitic line inductance can attribute to higher input voltage ripple. It is recommended to have a minimum of 400 μ F input capacitance for the MPT11220IL.

As the distance of the input power source to the input of the MPT11220IL is increased, it is recommended to increase input capacitance in order to mitigate the line inductance from the source. Low-ESR ceramic capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger capacitors in order to provide high frequency decoupling. Larger electrolytic or tantalum bulk capacitors may be used in conjunction to increase total input capacitance but should not be used solely as a replacement for the ceramic capacitors.

Output Capacitor Selection

The output ripple of a synchronous buck converter can be attributed to its inductance, switching frequency, and output decoupling. It is recommended to have a minimum of 1.0mF of output capacitance and up to 2mF for improved output ripple and load transient response for the MPT11220IL.

A combination of low ESR ceramic capacitors and POSCAP capacitors should be used. The dielectric must be X5R or X7R rated and the size must be at least 0805 (EIA) due to derating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

Application Information (Continued)

VRAMP Resistor Selection

The internal ramp generator can be adjusted for system stability by connecting a resistor between VRAMP and GND. Please see table below for Vramp Resistor values for setting Vramp amplitude:

| Vramp Voltage (VRAMP) | Vramp Amplitude | VRAMP Resistor (k Ω) |
|---|-----------------|------------------------------|
| $VRAMP < 1/16 * VDD$ | Vramp1 | 0.6 |
| $1/16 * VDD < VRAMP < 3/16 * VDD$ | Vramp2 | 1.42 |
| $3/16 * VDD < VRAMP < 5/16 * VDD$ | Vramp3 | 3.36 |
| $5/16 * VDD < VRAMP < 7/16 * VDD$ | Vramp4 | 6 |
| $VRAMP > 15/16 * VDD$ | Vramp1 | OPEN |
| Vramp level is: Vramp1 < Vramp2 < Vramp3 < Vramp4 | | |

Table 2: VRAMP Resistor values to set Vramp level

FADJ Resistor Selection

The Switching Frequency can be programmed to optimize efficiency and ripple currents over the various ranges for Vout and Vin. The MPT11220IL supports adjustable switching frequency from 600KHz to 1.2MHz. The switching frequency can be adjusted with a resistor between FADJ and GND. The RFADJ and FSW relationship is shown in table below, with 600 kHz Fsw is default with no resistor connected on FADJ:

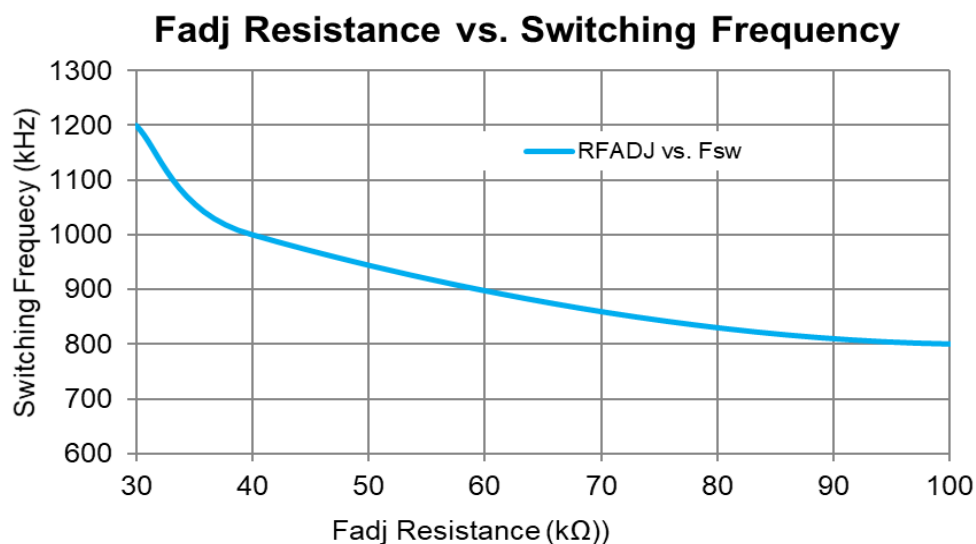


Figure 6: FADJ Resistance setting and associated switching frequency

IR Reflow Profile

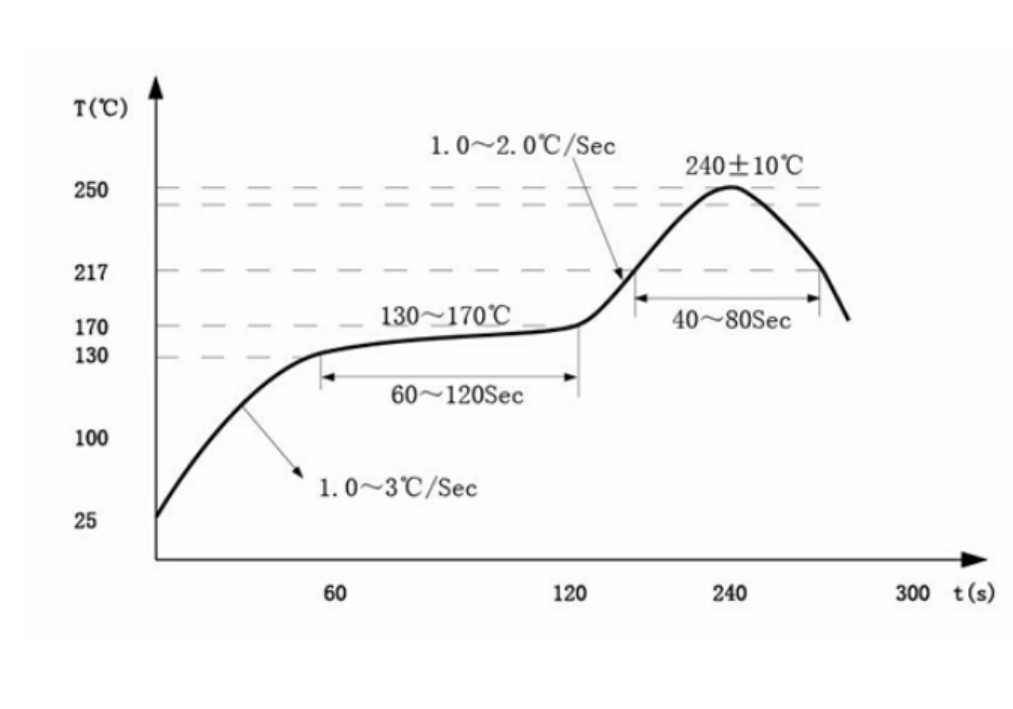


Figure 7: IR Reflow Profile for the 100-pin Open-Frame Package

Layout Recommendations

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the MPT11220IL package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The Input/Output Voltage and PGND traces between the capacitors and the MPT11220IL should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: In order to minimize the Power GND loop, it is recommended to route the input and output loops close to the same point, which is the ground of the MPT11220IL. Decoupling ceramic capacitors are to be placed as close as possible to the module in order to contain the switching noise in the smallest possible loops and to improve PVIN decoupling by minimizing the series parasitic inductance of the PVIN traces.

Recommendation 3: The large power thermal pads underneath the device must be connected to their respective planes through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1-oz. copper plating on the inside wall, making the finished hole size around 0.2mm to 0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 4: Multiple small vias (the same size as the thermal vias discussed in recommendation 3 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. Put the vias under the capacitors along the edge of the GND copper closest to the Voltage copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductance in the input and output current loops. If the vias cannot be placed under the C_{IN} and C_{OUT} , then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

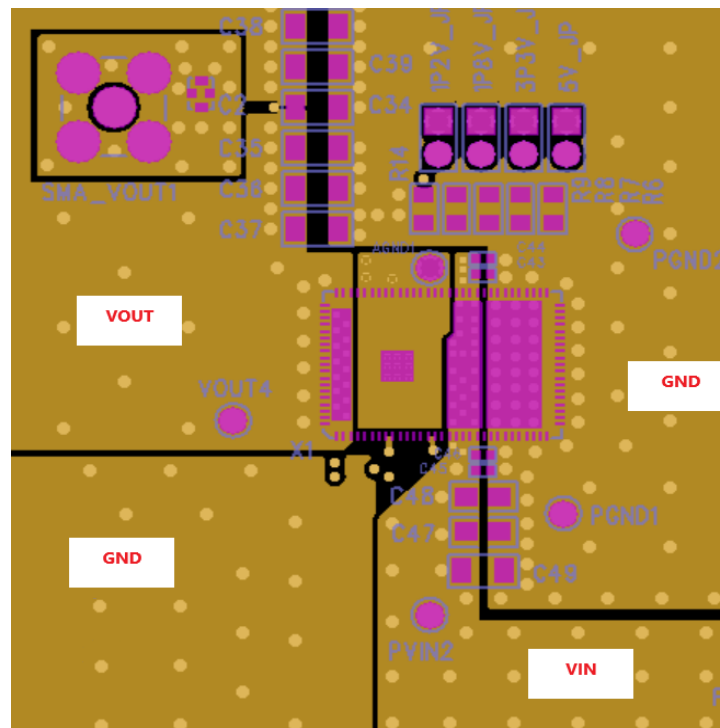


Figure 8: Illustration of Layout recommendations 1 to 4.

Layout Recommendations (Continued)

Recommendation 5: It is recommended that below the MPT11220IL module, the layers under the top layer should be solid ground planes. This will provide good shielding and lower the ground impedance at the top layer where the module is mounted. AGND should also be routed as a copper plane, in order to reduce the ground impedance.

Recommendation 6: It is highly recommended to use separate nets for AGND and PGND and connect them through a 0Ω resistor or a short. This will help prevent noise from the noisier Power Ground disturbing the more sensitive Analog Ground. The PGND connection point should be near the Output Capacitor GND termination as that GND point is not as noisy as the Input capacitor GND points.

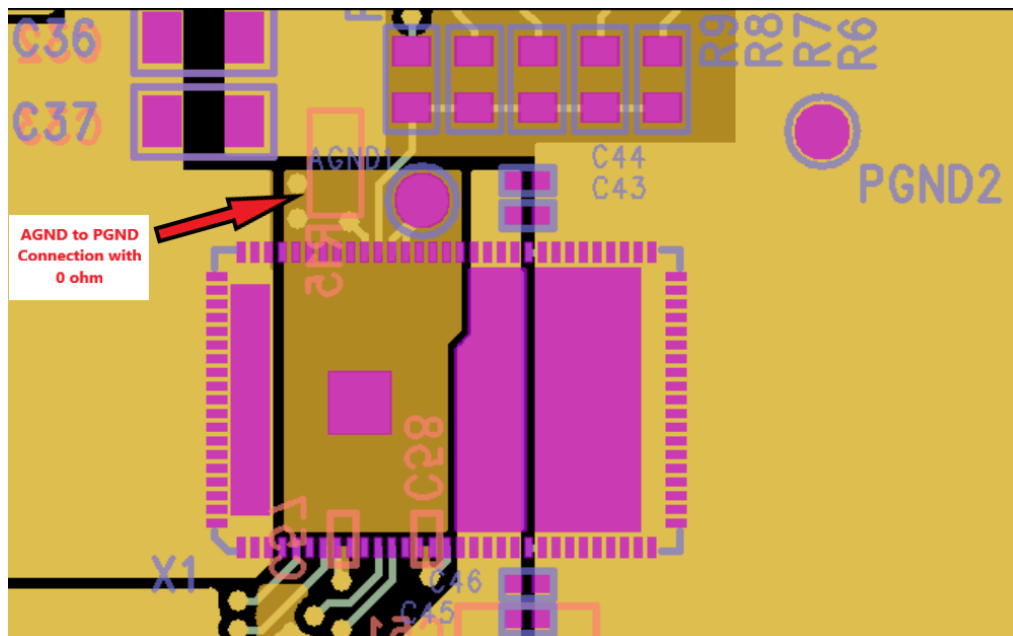


Figure 9: Illustration of Layout recommendations 6.

Recommendation 7: The V_{OUT} sense point should be connected at the last output filter capacitor furthest from the VOUT pins. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

Package drawings

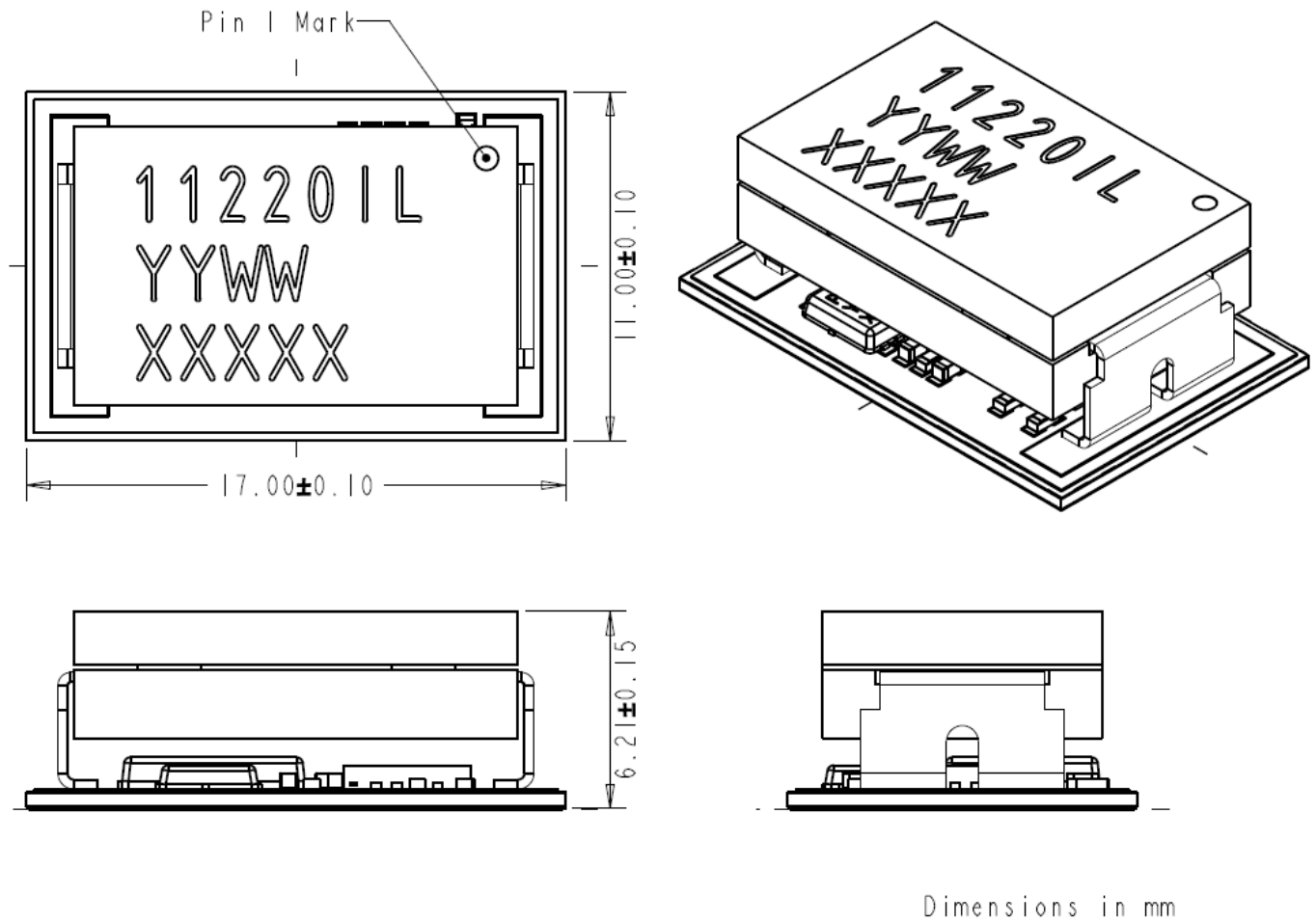


Figure 10: Open Frame Package Drawing

Design considerations for substrate based modules

Exposed Metal on Bottom of Device

All of the thermal pads and the perimeter pads are to be mechanically or electrically connected to the board. The PCB top layer under the MPT11220IL should be clear of any metal (copper pours, traces, or vias) except for the thermal pad.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package.

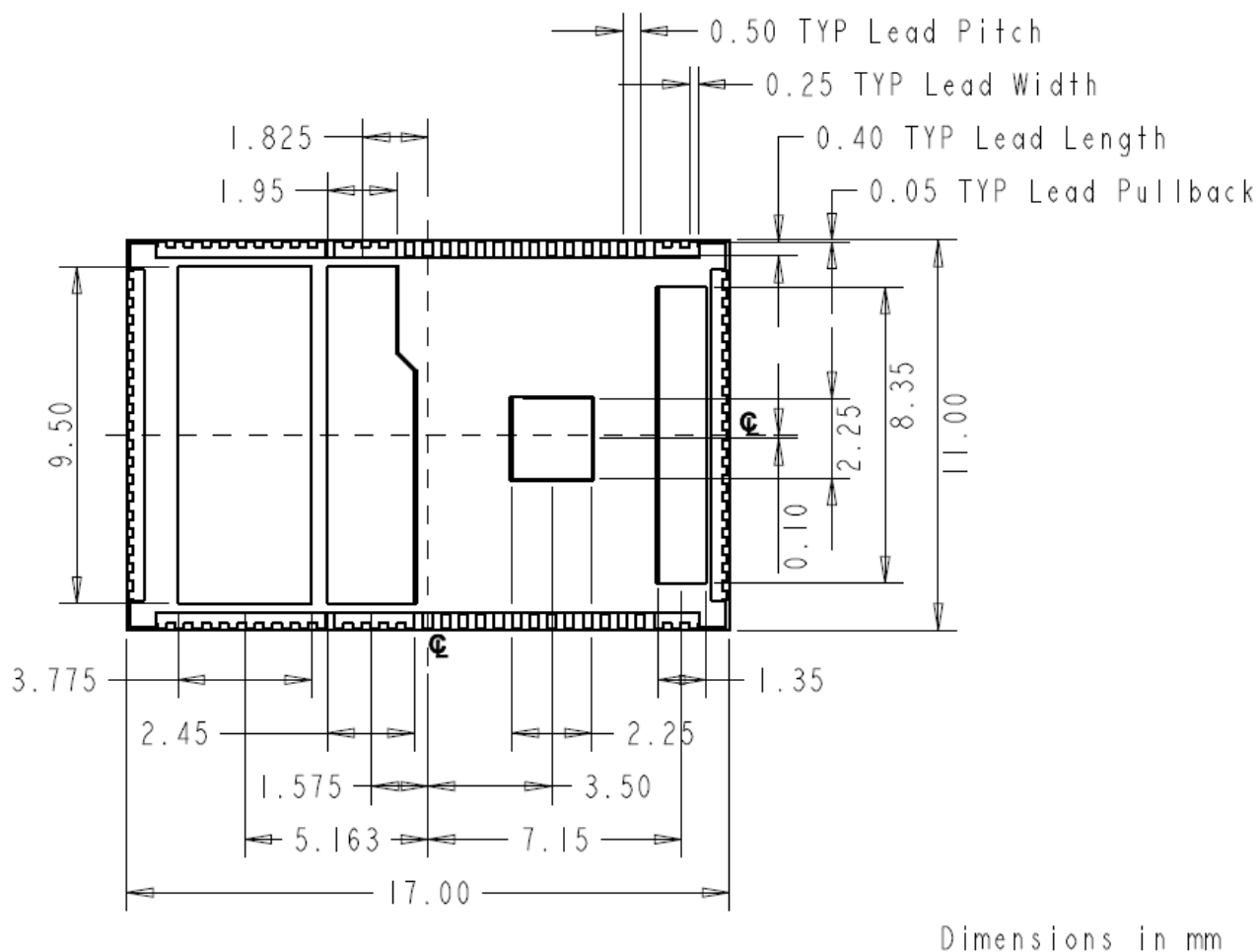
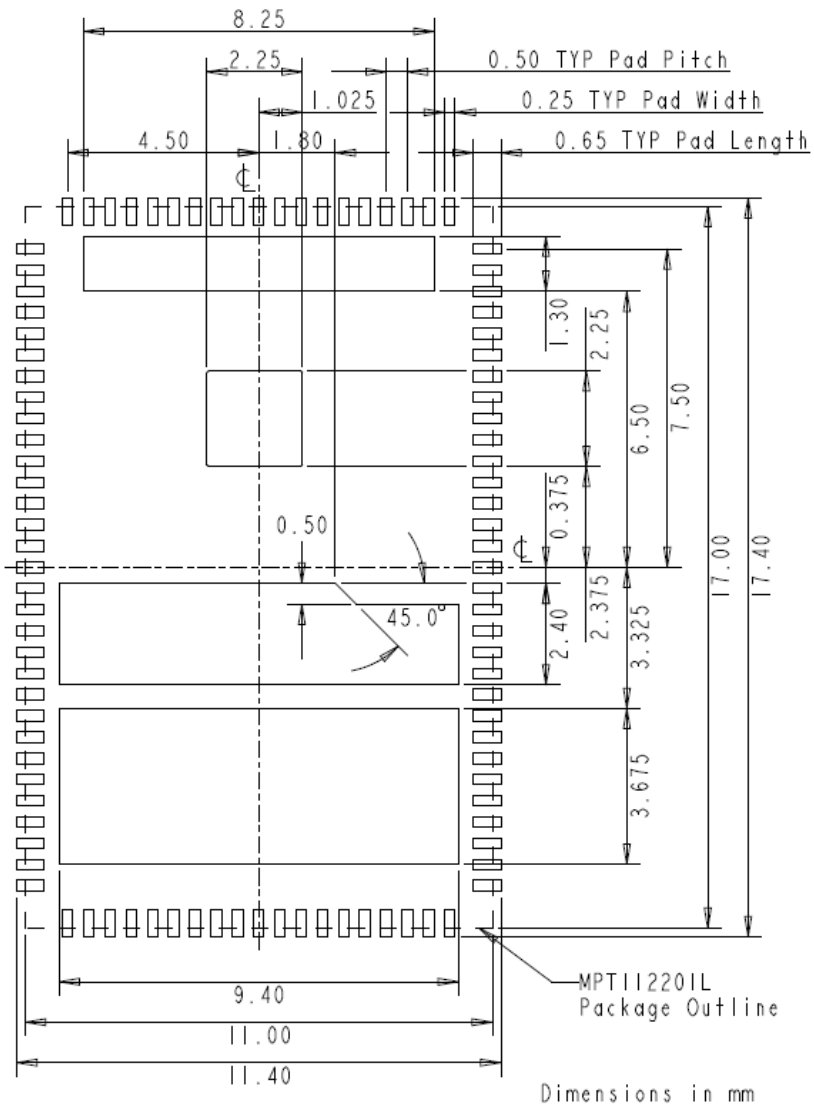


Figure 11: Open-Frame exposed metal (Bottom View)



Solder Stencil Information

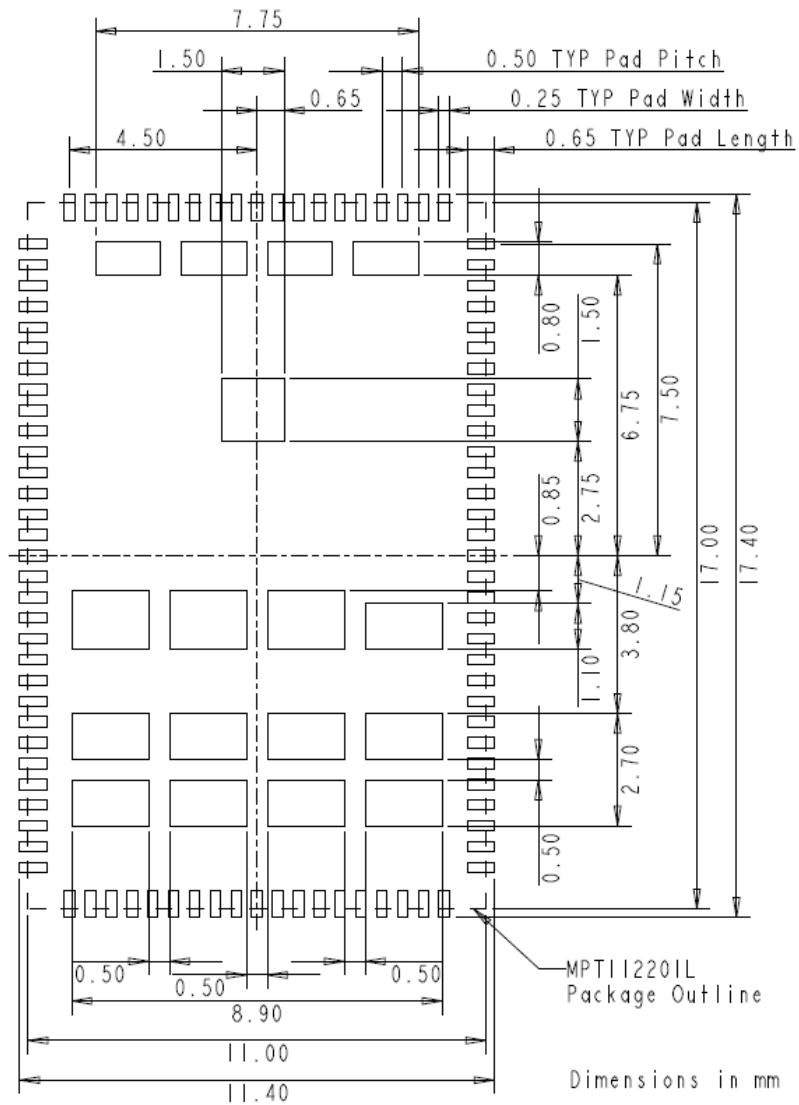


Figure 13: Recommended Solder Stencil opening dimensions